ABSTRACT OF THE DISCLOSURE

A method for forming a dual damascene structure for a semiconductor device, in accordance with the present invention, includes providing conductive regions on a first layer, forming an interlevel dielectric layer over the first layer and forming an etch stop layer over the interlevel dielectric layer. The etch stop layer includes a polymer material having a dielectric constant of less than about 3.0. The etch stop layer is patterned to form a via pattern, and a trench dielectric layer is deposited on the etch stop layer and in holes of the via pattern. Trenches are formed in the trench dielectric layer by etching the trench layer in accordance with a trench pattern, and vias are formed in the interlevel dielectric layer by etching through the trenches using the etch stop layer to self-align the trenches to the vias and expose the conductive regions on the first layer.